REMARKS:

This paper is herewith filed in response to the Examiner's Office Action mailed on March 24, 2008 for the above-captioned U.S. Patent Application. This office action is a rejection of claims 1-51 of the application, of which claims 25-38 are withdrawn from consideration.

More specifically, the Examiner has rejected claims 1-2, 5-14, 17-24, 39-40, and 43-50 under 35 USC 103(a) as being unpatentable over anticipated Young (US6,346,832) in view of Moyer (US6,566,911); and rejected claim 51 under 35 USC 103(a) as being unpatentable over the modified communication apparatus of Young in view of Moyer and further in view of Pena-Finol (US5,832,370). The Applicants respectfully traverse the rejection.

The Applicants note that claims 1-4, 13-16, and 39-42 have been amended for mere formality. Claims 52-54 have been added. Support for the new claims can be found at least on page 11 lines 15-22. No new matter is added.

Firstly, the Applicants disagree with the Examiner's statement in section 5 of the Office Action that "the Applicants [have] not presented concrete evidence for establishing "reasonable diligence to reduction to practice" as required by MPEP 2138.05-06." The Applicants note that section 2138.05-.06 appear to relate to Interferences.

It is noted that the earliest date for the reference Moyer sought to be disqualified as prior art against this Application is May 18, 2001. In the prior Response to Office action dated December 20, 2007 a Declaration under 37 USC 1.131 was submitted which shows an asserted date of conception at least as early as April 19, 2001 and an Exhibit B which independently proves the asserted date. Further, there was submitted Exhibit C which evidences that Nokia Corporation tasked the firm Harrington & Smith on May 18, 2001 to prepare and file a non-Provisional US Patent Application based on that subject matter. In addition, as submitted the Applicants assert that Exhibit D shows diligence in preparing the application during and up to September 2001. The application was filed on November 2, 2001.

As previously stated, caselaw holds that once an invention is submitted to an attorney for drafting of a patent application, diligence is satisfied when the attorney takes up work in a reasonable order. "[D]ecisions (as to the order in which a patent attorney prepares cases) recognize that the pressure of other business on a patent attorney may be a sufficient excuse for delay in filing provided the attorney takes up work in a reasonable order..." *Chisum on Patents*, vol 3, ch. 10.07[4][e] (Matthew Bender & Co., Inc., Rel. 82-3/02). Gould v. Schawlow, 150 USPQ 634 (CCPA 1966); Rines v. Morgan, 116 USPQ 145, 148 (CCPA 1957) ("it is not necessary that an inventor or his attorney should drop all other work and concentrate on the particular invention involved; and if the attorney has a reasonable backlog of work which he takes up in chronological order and carries out expeditiously, that is sufficient.").

In addition, it is noted that as cited by the Examiner MPEP 2138.06 under "DILIGENCE REQUIRED IN PREPARING AND FILING PATENT APPLICATION" states:

> "Reasonable diligence is all that is required of the attorney. Reasonable diligence is established if attorney worked reasonably hard on the application during the continuous critical period. If the attorney has a reasonable backlog of unrelated cases which he takes up in chronological order and carries out expeditiously, that is sufficient."

The undersigned asserts that based on a personal interview, the attorney preparing the case had a reasonable backlog of patent cases that he took up in a reasonable order during the entire period from May 18, 2001 to September 2, 2001. The undersigned attests that handwritten notes in the attorney's folder date the top communication at page 1 of Exhibit C as on July 5, 2001, and the filing attorney billed time in September and October of 2001. If further information is requested the Examiner is respectfully requested to provide such a request in a non-final Office Action.

As can be seen from the prior filed submissions, as stated above, the Invention was conceived as early as April 19, 2001 prior to the earliest date for the reference Moyer of May 18, 2001. The Attorneys were given instructions to file a non-Provisional Application of May 18, 2001. The Applicants submit that these facts as sworn to are seen to be sufficient to disqualify Moyer as a prior art against this Application. For at least the reasons stated the Examiner is respectfully requested to reconsider and disqualify Moyer.

However, although the Applicants do not agree with the Examiner's objection to a disqualification of Moyer, the Applicants submit that Young in view of Moyer still can not be seen to disclose or suggest at least claim 1.

Claim 1 as amended recites:

> "A multi-mode Input/Output (I/O) circuit for transmitting and receiving data between integrated circuits (ICs), wherein each IC contains at least one of said I/O circuits, comprising at least one of transmitter circuitry or receiver circuitry, said transmitter circuitry configured to send data to another IC, and said receiver circuitry configured to receive data from another IC, said I/O circuit being constructed with CMOS-based transistors that are selectively interconnected together by switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link."

In the rejection of claim 1 the Examiner states:

> "Young disclosed a multimode Input/Output circuit for transmitting and receiving data between integrated circuits wherein each IC having at least one of transmitter circuitry (fig. 1/no. 10) and receiver circuitry (fig. 1/no. 12), **that are selectively interconnected together by switches to operate as single-ended, voltage mode links, and as a single differential voltage mode link** (col. 4/In. 9-14)," (emphasis added).

The Applicants note that Young relates to a transmission circuit in which a high speed differential signal and a common mode signal are sent over the same two lines. Further, as cited Young discloses:

> "Thus, the transmission and receive circuits shown in FIG. 1 provide both a high speed differential signal and **a common mode signal which is utilized as a single-ended input for single-ended amplifier 32**," (col. 4, lines 9-12).

The Applicants note that here Young merely discloses that the common mode signal sent with the differential signal is utilized as an input for a single ended amplifier. Further, as admitted by the Examiner in the rejection Young does not disclose or suggest **two single-ended** which can be either current or voltage mode links. The Applicants submit that Young can not be seen to relate to selectively interconnecting a circuit to operate as **two**

single-ended, current or voltage mode links, and as a single differential current or voltage mode link as in claim 1.

The Applicants note that in the rejection of claim 1 the Examiner states:

> "Young disclosed such pair of conductor being utilized as single-ended mode **but not explicitly as two single-ended modes**. However, **Moyer suggested such method (abstract)**. Therefore, it would have been obvious to one of ordinary skill in the art to provide such switching mode, as taught by Moyer, to the Multi-Channeling Apparatus of Young in order provide a flexible interface signaling for an integrated circuit and save cost," (emphasis added).

The Applicants disagree with the Examiner. Further, the Applicants respectfully reassert, for at least the reasons already stated, that Moyer is not seen to be qualified as prior art against the application. However, even if Moyer were qualified as prior art against the application, which is not agreed to, the Applicants contend that Moyer can not be seen to relate to **two single-ended, current or voltage mode links, and a single differential current or voltage mode link** as in claim 1.

The Applicants note that Moyer discloses

> "In one mode, **cell 100 outputs signaling compatible with Reduced Swing Differential Signaling (RSDS, a trademark of National Semiconductor Corp., as described in RSDS™** Specification, Rev. 0.95, May 2001). When driven into a 100-ohm load placed across PAD0 and PAD1, the differential voltage across the pads will be roughly 250 mV, with an offset voltage V.sub.off of approximately V.sub.ref =1.3 V," (emphasis added), (col. 3, lines 55-67).

Here it can be seen that Moyer discloses using, trademark identified **Reduced Swing Differential Signaling** method to perform the differential signaling of Moyer. The Applicants submit that Moyer can not be seen to disclose or suggest two single-ended, **current or voltage mode links** and a single differential **current or voltage mode link** as in claim 1.

Moyer, further discloses:

> "In differential output mode, [...] Signal IREF provides a reference current I_0 for generating an appropriate **RSDS current level**, and signal VREF provides a reference voltage for generating an appropriate **RSDS bias voltage**," (emphasis added), (col. 4, lines 19-27).

The Applicants submit that the RSDS signaling in Moyer appears to relate to generating an appropriate RSDS current level and an appropriate RSDS bias voltage. Thus, it is unclear in Moyer whether such a signaling method can even be applied as used in a voltage or current mode link. The Applicants submit that here Moyer appears to disclose a type of hybrid link. The Applicants contend that Moyer can not be seen to disclose or suggest a current or voltage mode link as in claim 1. The Applicants can not find in all of Moyer where Moyer can be seen to disclose or suggest two single-ended, **current or voltage mode links** and a single differential **current or voltage mode link** as in claim 1.

The Applicants contend that for at least the reasons stated even if Young were modified in view of Moyer, which is not agreed to as proper, the modification would still not disclose or suggest claim 1. Thus, the rejection of claim 1 should be removed.

Further, the Applicants submit that for at least the reasons that independent claims 13 and 39 recite language similar to claim 1 as stated above, the references cited can not be seen to disclose or suggest these claims.

Further, in regards to claim 52 neither the Applicants contend that the references cited are not seen to disclose or suggest where claim 52 recites "**where in the single differential current mode a current drawn from the at least one of the transmitter or receiver circuitry is constant.**"

In addition, as the claims 53 and 54 recite language similar to claim 52 the references cited are not seen to disclose or suggest these claims.

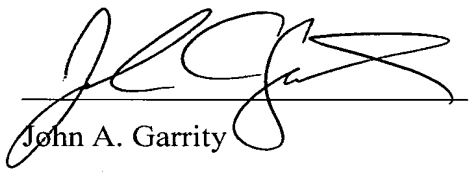
The Applicants note that although not all the rejections in the Office Action are argued, the Applicants do not acquiesce to these rejections.

In addition, claims 2-12, 14-24, and 40-51 are seen to overcome the rejections for at least the reason that they depend from claims 1, 13, and 39, respectively.

Based on the above explanations and arguments, it is clear that the references cited cannot be seen to disclose or suggest claims 1-24 and 39-54. The Examiner is respectfully requested to reconsider and remove the rejections of claims 1-24 and 39-54 and to allow all of the pending claims 1-24 and 39-54 as now presented for examination.

For all of the foregoing reasons, it is respectfully submitted that all of the claims now present in the application are clearly novel and patentable over the prior art of record. Should any unresolved issue remain, the Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted:



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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450.

July 24, 2008 — Date

Name of Person Making Deposit